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SAXENA, AKASH	

ART UNIT	PAPER NUMBER
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NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/673,507	STRANG, ERIC J.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-81* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-81* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/5/07*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-81 has/have been presented for examination based on amendment filed on 17th December 2007.
2. Claim(s) 1, 38 and 75 is/are amended.
3. Claim(s) 1-81 remain rejected under 35 USC § 112.
4. Based on the amendment in the alternative, claims 1, 8 and 75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sonderman, in view of Jain, further in view of Tan.
5. Claim(s) 1-81 remain rejected under 35 USC § 103 as previously presented.
6. Claims 1-21, 29-30, 32-34, 37, 38-58, 66-67, 69-71, and 74 were rejected with combination of Sonderman & Jain.
7. Claims 22 and 59 were rejected with combination of Sonderman, Jain and Yunemura.
8. Claims 23-28 and 60-65 were rejected with combination of Sonderman, Jain and Chen.
9. Claims 31, 36, 68 and 73 were rejected with combination of Sonderman, Jain and Nikoonahad.
10. Claims 35 and 72 were rejected with combination of Sonderman and Fatke.
11. The arguments submitted by the applicant have been fully considered. Claims 1-81 remain rejected and this action is made FINAL. The examiner's response is as follows.

Information Disclosure Statement

12. Applicant had filed two non-patent literature documents containing an office actions mailed by Chinese patent.office dated 11/5/2007 and 12/17/2007. It has been placed in the application file, but the information referred to therein has not been considered as to the merits because the documents are not listed on the IDS.

Response to Applicant's Remarks for 35 U.S.C. § 112¶1st

13. Applicant has amended new limitations "said first principles simulation result being produced in a time frame shorter in time than the actual process being performed,", however this does not cure the deficiency pointed out in the enablement rejection made in the previous office action.

Applicant has quoted specification *pg.7-8 numbered paragraphs [0035] and [0036]*. These paragraph are not enabling, although they rely on the commercially available packages to model the various first principle simulation models, the details of the model are absent from the specification. The details of these model which lead to unexpected results are very relevant to the designing the first principle physical model. Examiner respectfully maintains the rejection.

As per arguments made for claims 6-9, these claims do not disclose how the first principle model is conceived and implemented making it faster. Arguendo, even if they cure the deficiency of claim 1 they are dependent from claim 1 and claim 1 itself would still be rejected as non-enabling.

As per arguments made for claims 15-19 and 79, using distributed simulation to address the enablement for the first principle simulation is not found to be persuasive.

Response to Applicant's Remarks for 35 U.S.C. § 103

(Argument 1) Applicant has argued in Remarks Pg.23-24:

> Yet, Applicant respectfully points out that, at col. 9, lines 46-51, Sonderman et al specifically states:
>
> > *The system 100 then optimizes the simulation (described above) to find more optimal process target (Ti) for each silicon wafer, Si to be processed. These target values are then used to generate new control inputs, XTi, on the line 805 to control a subsequent process of a silicon wafer Si. [Emphasis added]*
>
> The plain reading of this section of Sonderman et al is that the system 100 then (e.g., at time T1) optimizes the simulation for each silicon wafer, Si to be processed (e.g., later at time T2). In other words, the simulation results of Sonderman et al produce a new control input for each silicon wafer to be processed. Thus, <u>*Applicant respectfully submits that Sonderman et al teach performing first principles simulation for the actual process to be performed before performance of the actual process*</u>, and not the claimed <u>*performing first principles simulation for the actual process being performed during performance of the actual process*</u>.

(Response 1) Sonderman Col.4 Line 65-Col.5 Line 10 states:

> Furthermore, the simulation environment 210 can be used for feedback modification of control parameters invoked by the process control environment 180. <u>For example, the manufacturing environment 170 can send metrology data results into the simulation environment 210. The simulation environment 210 can then use the metrology data results and perform various tests and calculations to provide more accurate, modified control parameters to the process control environment 180.</u> A feedback loop in then completed when the process control environment 180 sends the modified or adjusted process control parameters to the manufacturing environment 170 for further processing of semiconductor wafers.

Sonderman clearly teaches inputting process data relating to an actual process being performed by the semiconductor processing tool, into the simulator and applying the simulation result to the semiconductor-processing tool. Sonderman col. 9, lines 46-51 above teaches using the simulation result subsequent process of the same wafer. Sonderman teaches performing interaction concurrently between the simulation environment (first principle simulation) and the semiconductor-processing tool (Sonderman: Fig.2; Col.4 Lines 48-63). Sonderman does not teach that

simulation happens consecutively as alleged by applicant. ~~Examiner would appreciate if applicant can point out section in Sonderman for this conclusion.~~ MK.

Arguendo, even if applicant statement that Sonderman does not teach *performing first principles simulation for the actual process being performed during performance of the actual process* is true, applicant alleges that the simulation completes faster than the actual process, with the intent that the results of the simulation can be used in assisting the actual process. It is clear that the simulation will start at T1 and finish at T2 at which point the results can be applied to the actual processing subsequent to the time T2. Hence the teaching present in Sonderman col. 9, lines 46-51 reads on this interpretation as well.

(Argument 2) Applicant has argued in Remarks Pg. 24:

> In the last filed response, Figure 4 of Sonderman et al was pointed out for clearly showing that **the simulation results are produced ahead of performing a process** and thus have to be based on historical data, and **not based on the actual process being performed during performance of the actual process**.

(Response 2) As to reference made to Fig.4, Sonderman Col.6 Lines 35-47 states:

> Once the system 100 performs the process simulation function, the system 100 performs an interfacing function, which facilitates interfacing of the simulation data with the process control environment 180 (block 430). The process control environment 180 can utilize the simulation data in order to **modify** or **define manufacturing control parameters** that control the actual processing steps performed by the system 100. Once the system 100 interfaces the simulation data with the process control environment 180, the system 100 then performs a manufacturing process based upon the manufacturing parameters defined by the process control environment 180 (block 440).

There is no indication that the actual process was **not** ongoing when the simulation was being performed in teaching above. The fact that simulation results are use to ***modify*** manufacturing control parameter indicate contrary to applicant's allegation. The interfacing step may be sequential at best. Please see the timeline below of examiner's interpretation.

Time T1: Actual ongoing process with predefined **<u>manufacturing control parameters</u>**. (See Col.4 Line 65-Col.5 Line 9).

Simulation starts with predefined control parameters.

Time T2:

Simulation finishes.

Time T3:

Simulation results **<u>interfaced</u>** with the actual process.

Time T4:

<u>The process control environment 180 can utilize the simulation data in order to **modify manufacturing control parameters.**</u>

The simulation in Sonderman et al is happening concurrently to the actual process.

Also See Sonderman: Col.4 Line 65-Col.5 Line 9.

(Argument 3) Applicant has argued in Remarks Pg.26:

> Yet, Applicant respectfully points out that this description in Sonderman et al is a description of feedback modification of control parameters. Feedback modification is by definition the control of future wafers based on what has already occurred to a previous wafer. Hence, this section supports rather than refutes Applicant's position on this matter.
>
> Accordingly, Applicant respectfully submits that Sonderman et al do not disclose and indeed ***<u>teach away</u>*** from the present invention where data input from an actual process being performed is used for producing a first principles simulation result, which is produced for the actual process being performed during performance of the actual process.

(Response 3) The argued teaching in Sonderman Col.4 Line 65-Col.5 Line 9 states:

> Furthermore, the simulation environment 210 can be used for feedback modification of control parameters invoked by the process control environment 180. For example, the manufacturing environment 170 can send metrology data results into the simulation environment 210. The <u>simulation environment 210 can then use the metrology data results</u> and perform various tests and calculations to provide more accurate, modified control parameters to the process control environment 180. <u>A feedback loop in then completed when the process control environment 180 sends the **modified or adjusted process control parameters to the manufacturing environment 170 for further processing of semiconductor wafers [1].**</u>

This passage is used to show that with an ongoing actual process the simulation is provided the input as well as the current state of the ongoing process to perform further simulation and correct the actual process. Nowhere in the teaching does it state the corrected simulation results are not used for the current ongoing process **[1].** As shown above the Sonderman does not teach away, rather it clearly

demonstrates that simulation is used concurrently to modify and assist the ongoing actual manufacturing process. Examiner finds applicant's argument unpersuasive.

(Argument 4) Applicant has argued in Remarks Pg.26:

> Lastly, with regard to Sonderman et al, Sonderman et al do not disclose that a simulation result is produced in a time frame shorter in time than the actual process being performed, as presently defined in the independent claims.

(Response 4) First, this newly amended limitation is known in the art and is presented in the background section of the specification Pg. 2 [0004] as:

> [0004] These industry and manufacturing challenges have led to interest in more use of computer based modeling and simulation in the semiconductor manufacturing industry. Computer-based modeling and simulation are increasingly being used for prediction of tool performance during the semiconductor manufacturing tool design process. The use of modeling allows the reduction of both cost and time involved in the tOol development cycle. Modeling in many disciplines, such as stress, thermal, magnetics, etc., has i:eached a level-of maturity where it can be trusted to provide accurate answers to design questions. Moreover, computer power has been increasing rapidly along with the development of new solution algorithms, both of which resulted in reduction of time required to obtain a simulation result**. Indeed, the present inventors have recognized that a large number of simulations typically done in the tool design stage can presently be run in times comparable to wafer or wafer cassette processing times.** These trends have led to the suggestion that simulation capability typically used only for tool design can be implemented directly on the tool itself to aid in various processes performed by the tool. For example, the 2001 International Technology Roadmap for Semiconductors identifies issues impeding the development of on-tool integrated simulation capability as an enabling technology for manufacturing very small features in future semiconductor devices.

Further evidence can be found as far back as in IEEE 1990 paper by Su-shing Chen, "AEMPES: An expert system for in-situ diagnostics and process monitoring" addressing the on-tool simulation (as disclosed in specification [0004]) as well as resource utilization problem (as disclosed in specification [0005]).

Furthermore, in simulation the time frame is set by user and depends upon time resolution. One would want it to be faster than the process or otherwise it will lag the "actual process" and therefore defeat the purpose of concurrent simulation, the

results of which are used to drive the process, as shown in Sonderman Fig.2 & Col.4 Line 65-Col.5 Line 9.

Examiner finds the applicant's argument unpersuasive.

(Argument 5) Applicant has argued that Jain does not overcome the deficiencies of Sonderman.

(Response 5) Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Applicant has merely cited portion of Jain without clearly showing why Jain does not overcome the deficiencies of Sonderman.

(Argument 6) Applicant has stated the following:

> Moreover, the proposed development work in Jain is understood better in the light of the "conventional approach" referred to by Kee et al, made of record by the Information Disclosure Statement filed December 20, 2005.

Further arguments are presented with current case law KSR International Vs. Teleflex Inc.

(Response 6) First, Kee et al is not used as prior art for rejecting the current invention. Secondly, examiner fails to see the connection between Jain and Kee et al as neither of them reference to each other in any way. Thirdly, Applicant also has not further established why the so-called "conventional approach" would link them. In light of the above applicant's arguments are found to be unpersuasive. Kee is irrelevant to merits of rejection. Applicants allege it is rebuttal evidence, but actually treat Kee as applied art, then argue against the hypothetical combination using KSR.

Even if Kee typifies state of art, it speaks to state of art in **1994**, **not 2001**, filing date of Sonderman. Kee is not "rebuttal" evidence and in fact is evidence of nothing. Kee is not considered.

(Argument 7) Applicant has argued:

> In the present situation, the claimed method of performing a first principles simulation for the actual process being performed during performance of the actual process produces more than an expected result in that Sonderman et al (***in having to develop a new control inputs for each subsequent wafer***) can not compensate for real time excursions from the existing model occurring while the wafer is being processed. In other words, the lengthy time for generation of a first principles model simulation in the prior art prevents one from realizing a real time process control based on a first principles simulation during the actual process. Indeed, as pointed out above, the examiner considered it an impossibility to simultaneously perform a first principles simulation result and to control the actual process being run with the first principles simulation result. Hence, the claimed processes and systems produce an unexpected result.

(Response 7) Examiner thanks applicant for the remarks above, however the new control inputs are not developed for the processing of each subsequent wafer, but instead are for subsequent processing [performed on] a silicon wafer S.sub.i (Sonderman: Col.9 Lines 44-46 – this point is also addressed above in response to argument 1).

Further ***most importantly*** what makes the current first principle simulation model realize the real time process control possible is not claimed. Further distinguishing it from Sonderman may also help in defining a more patentable subject matter.

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Claim Rejections - 35 USC § 112¶1st

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

14. Claim 1-81 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Exact details of what basic physical and chemical attribute of the semiconductor processing tool are used to construct a first principle simulation model which is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

    Applicant has quoted specification paragraphs [0035] and [0036]. These paragraph are not enabling, although they rely on the commercially available packages to model the various first principle simulation models, the details of the model are absent from the specification. The details of these model which lead to unexpected results are very relevant to the designing the first principle physical model. Examiner respectfully maintains the rejection.

Response to Applicant's Remarks for Double Patenting

15. Applicant's arguments relating to filing a terminal disclaimer for applications 10/673,501, 10/673,507 and 10/673,583 are considered and double patenting rejection is maintained until a terminal disclaimer is filed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

16. Claims 1, 8 and 75 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (<u>Sonderman</u> hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (<u>Jain</u> hereafter) further in view U.S. Patent No. 6,263,255 issued to Tan et al (<u>Tan</u> hereafter).

<u>Regarding Claim 1 (New *1/29/08*)</u>

Sonderman teaches a method to controlling a process performed by a semiconductor-processing tool (Sonderman: Summary, at least in Col.2 Lines 10-17;Col.3 Lines 45-49) by inputting *process* data relating to *an actual* process *being* performed by the semiconductor-processing tool (Sonderman: at least in Col.3 Lines 50-67; *Col.7 Lines 8-20*). Further, Sonderman teaches inputting the first principle physical model relating to the semiconductor-processing tool *describing at least one of a basic physical or chemical attributes* (Sonderman: at least in Col.5 Lines 11-17; 49-67) as device physics model, a process model and an equipment model. Further, Sonderman teaches performing first principle simulation *for the actual process being performed* during performance of actual process *(Sonderman: Col.7 Lines 4-7; Col.3 Lines 56-63,* Fig.1-3*)* using the physical model to *provide simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed* (Sonderman: at least in Col.5-7). Further, Sonderman teaches using the first principle simulation results *obtained during the performance of the actual process* (Sonderman: Fig. 1-3 *Col.7 Lines 4-7;*

Col.3 Lines 56-63) to control the process performed by the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 48-64; Fig.1-8; Col.2 Lines 10-17).

Sonderman does not teach first principle model including a set of computer encoded differential equations.

Jain teaches computer encoded differential equations using MPE engine, which can be applied to wafer processing (Jain: Abstract). Jain also teaches dedicated and wafer level implementation of MPE engine to provide enhanced performance (Jain: Pg. 372 Section V Dedicated MPE).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Jain to Sonderman to solve differential equation for the semiconductor processing tool. Sonderman teaches building various models, which work in real-time feedback control simulating actual semiconductor modeling process (Sonderman: Fig.1; Col.7 Lines 8-20), while Jain makes possible by providing model-solving capacity in real time when differential equations are present in the model (like thermal patterns in semiconductor wafer model) (Jain: Abstract).

Arguendo, even if Sonderman and Jain do no explicitly teach said first principles simulation result being produced in a time frame shorter in time than the actual process being performed Tan teach the above limitation.

<u>Tan teaches said first principles simulation result being produced in a time frame shorter in time than the actual process being performed</u> as in Col.2 Lines 7-12 as:

(4) Model-based real-time process control using in situ inputs, process models, and process control strategies to correctly process control parameters during the process run, ensuring that product characteristics are achieved.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Tan to Sonderman to facilitate the simulation as defined in Fig.2. The motivation to combine is that both Tan and Sonderman teach performing simulation of semiconductor assembly line including the tools and the processes running on them (Tan: Col.5 Line 63-Col.6 Line 8; Sonderman: Sonderman: Col.7 Lines 4-7; Col.3 Lines 56-63, Fig.1-3).

Regarding Claim 38 (New 1/29/08)

System claim 38 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 75 (New 1/29/08)

System claim 75 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

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17. Claims 1-21, 29-30, 32-34, 37, 38-58, 66-67, 69-71, and 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter).

Regarding Claim 1 (Updated 1/29/08)

Sonderman teaches a method to controlling a process performed by a semiconductor-processing tool (Sonderman: Summary, at least in Col.2 Lines 10-17;Col.3 Lines 45-49) by inputting *process* data relating to *an actual* process *being* performed by the semiconductor-processing tool (Sonderman: at least in Col.3 Lines 50-67; *Col.7 Lines 8-20*). Further, Sonderman teaches inputting the first principle physical model relating to the semiconductor-processing tool *describing at least one of a basic physical or chemical attributes* (Sonderman: at least in Col.5 Lines 11-17; 49-67) as device physics model, a process model and an equipment model. Further, Sonderman teaches performing first principle simulation *for the actual process being performed* during performance of actual process *(Sonderman: Col.7 Lines 4-7; Col.3 Lines 56-63,* Fig.1-3*)* using the physical model to *provide simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed* (Sonderman: at least in Col.5-7), *said first principles simulation result being produced in a time frame shorter in time than the actual process being performed (Sonderman: Col.4 Lines 47-Col.5 Lines 10)*. Further, Sonderman teaches using the first principle simulation results

obtained during the performance of the actual process (Sonderman: Fig. 1-3 *Col.7 Lines 4-7; Col.3 Lines 56-63*) to control the process performed by the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 48-64; Fig.1-8; Col.2 Lines 10-17).

Sonderman does not teach first principle model including a set of computer encoded differential equations.

Jain teaches computer encoded differential equations using MPE engine, which can be applied to wafer processing (Jain: Abstract). Jain also teaches dedicated and wafer level implementation of MPE engine to provide enhanced performance (Jain: Pg. 372 Section V Dedicated MPE).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Jain to Sonderman to solve differential equation for the semiconductor processing tool. Sonderman teaches building various models, which work in real-time feedback control simulating actual semiconductor modeling process (Sonderman: Fig.1; Col.7 Lines 8-20), while Jain makes possible by providing model-solving capacity in real time when differential equations are present in the model (like thermal patterns in semiconductor wafer model) (Jain: Abstract).

Regarding Claim 2

Sonderman teaches directly inputting the *process* data relating to the *actual* process *being* performed by the semiconductor-processing tool from at least one of physical sensor (e.g. Scatterometry data, overlay data, dimensional data) and a metrology

tool physically mounted on the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 31-48; Col.4-8; Fig.1, 7; *Col.7 Lines 8-20*).

Regarding Claims 3-5

Sonderman teaches indirectly inputting the *process* data relating to the *actual* process performed by the semiconductor-processing tool from one of the manual input devices and a database as manual fashion data retrieval and automatic data retrieval; inputting data recorded from the previous run; inputting the data set by a simulation operator (Sonderman: at least in Fig.1-3 Col.1; Col.4-7; Col.7 Lines 8-20).

Regarding Claims 6-9

Sonderman teaches inputting process data relating to at least one of the physical characteristics of the semiconductor-processing tool and semiconductor tool environment, data relating to at east on of the characteristics and a result of a process performed by the semiconductor processing tool; inputting a spatially resolved model (as modified models) of the geometry of the semiconductor processing tool; inputting fundamental equations necessary to perform first principle simulation for the desired simulation result (Sonderman: at least in Col.5 Lines 10-18; Col.6 Lines 48-63; Col.9 (equations); Col.5-9; Fig 1-3; Col.7 Lines 8-20). Sonderman and Jain teach inputting fundamental equations as the set of computer encoded differential equations (Sonderman: Col.9 (equations); Jain: Pg. 372 Section V Dedicated MPE, Abstract).

Regarding Claim 10

Sonderman teaches performing interaction concurrently between the simulation environment (first principle simulation) and the semiconductor-processing tool (Sonderman: Fig.2; Col.4 Lines 48-63).

Regarding Claims 11-13

Sonderman teaches performing first principle simulation independent of the process performed by the semiconductor-processing tool; inputting data from to set initial & boundary condition on the first simulation model (Sonderman: at least in Col.5-8; Fig.3-4).

Regarding Claim 14

Sonderman teaches using the first principles simulation result comprises using the first principles simulation result to perform at least one of detecting, and classifying a fault in the process performed by the semiconductor-processing tool (Sonderman: at least in Col.5 Line 56 – Col.6 Line 24).

Regarding Claims 15-19

Sonderman teaches using a network of interconnected resources *inside the semiconductor manufacturing facility (Sonderman: Semiconductor tools on the factory floor – Col.9 Lines 60-65*) to perform *first principle simulation (Jain: Section III*); using code parallelization among interconnected computational resources to share the computational load of the first principle simulation; sharing simulation information among the interconnected resources to facilitate a process by the semiconductor-processing tool; sharing simulation results among the interconnected

resources to reduce redundant execution of substantially similar first principle simulation by different resources; sharing information comprising model changes among the interconnected resources to reduce the redundant refinements of first simulation by different resources (Sonderman: Fig.1-3, computer code software is described in Col.9 Lines 58 onward; Col.5-8).

Regarding Claims 20-21

Sonderman teaches remote access to computational and storage resources (Sonderman: Col.9 Line 58-Col.10 Line 31) where in wide area network is art inherent.

Regarding Claim 29

Sonderman teaches performing a principle components analysis to determine a relationship between spatial components of said first principles simulation result for the semiconductor processing tool and a set of at least one control variable, said relationship utilized to determine a correction to said set of at least one control variable in order to affect a reduction in the magnitude of said spatial components (Sonderman: Col.5 Line 56 – Col.6 Line 23).

Regarding Claim 30

Sonderman teaches first principle simulation controlling at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (Sonderman: at least in Col 4 Lines 18-31; Col.3 Lines 45-49).

Regarding Claim 32

Sonderman teaches inputting various parameters *as tool data* relating to etching, deposition etc. (Sonderman: at least in Col.5 Lines 56-67).

Regarding Claim 33

Sonderman teaches inputting physical geometric data as parameters for the equipment model where the equipment could be at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (Sonderman: Col.5 Lines 56-67).

Regarding Claim 34

Sonderman teaches first principles simulation result controlling the semiconductor processing tool by using model output to adjust said process performed by the semiconductor processing tool (Sonderman: Col.4 Lines 48-64; Fig.1-2).

Regarding Claim 37

Sonderman teaches inspecting process results and providing input to the first principles simulation for calibration purposes (Sonderman: Col.6 Lines 14-24).

Regarding Claim 38

System claim 38 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 39

System claim 39 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claims 40-42

System claims 40-42 disclose similar limitations as claims 3-5 and are rejected for the same reasons as claims 3-5 respectively.

Regarding Claims 43-46

System claims 43-46 disclose similar limitations as claims 6-9 and are rejected for the same reasons as claims 6-9 respectively.

Regarding Claim 47

System claim 47 discloses similar limitations as claim 10 and is rejected for the same reasons as claim 10.

Regarding Claims 48-50

System claims 48-50 disclose similar limitations as claims 11-13 and are rejected for the same reasons as claims 11-13 respectively.

Regarding Claim 51

System claim 51 discloses similar limitations as claim 14 and is rejected for the same reasons as claim 14.

Regarding Claims 52-56

System claims 52-56 disclose similar limitations as claims 15-19 and are rejected for the same reasons as claims 15-19 respectively.

Regarding Claims 57-58

System claims 57-58 disclose similar limitations as claims 20–21 and are rejected for the same reasons as claims 20-21 respectively. *Change in dependency from claim 52 to claim 38 of claim 57. is noted.*

Regarding Claim 66

System claim 66 discloses similar limitations as claim 29 and is rejected for the same reasons as claim 29.

Regarding Claim 67

System claim 67 discloses similar limitations as claim 30 and is rejected for the same reasons as claim 30.

Regarding Claim 69

System claim 69 discloses similar limitations as claim 32 and is rejected for the same reasons as claim 32.

Regarding Claim 70

System claim 70 discloses similar limitations as claim 33 and is rejected for the same reasons as claim 33.

Regarding Claim 71

System claim 71 discloses similar limitations as claim 34 and is rejected for the same reasons as claim 34.

Regarding Claim 74

System claim 74 discloses similar limitations as claim 37 and is rejected for the same reasons as claim 37.

<u>Regarding Claim 75 (Updated)</u>

System claim 75 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

<u>Regarding Claim 76 (Updated)</u>

System claim 76 discloses similar limitations as claim 16 and is rejected for the same reasons as claim 16. Sonderman teaches sharing *<u>inside the semiconductor device manufacturing facility (Sonderman: Semiconductor tools on the factory floor – Col.9 Lines 60-65</u>*) the computational load (also see APC).

<u>Regarding Claim 77</u>

System claim 77 discloses similar limitations as claim 17 and is rejected for the same reasons as claim 17.

<u>Regarding Claim 78 (Updated)</u>

Article of manufacture claim 78 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

<u>Regarding Claims 79-81</u>

Jain teaches use of Navier Stokes and other known simulation solutions for solving various simulation problems as initial condition (Jain: Pg. 367-368 Section "Governing Rationale" Sub-Section A. Governing Equations). Sonderman also teaches initializing the models with input data (Sonderman: Col.7 Lines 8-20).

18. Claims 22 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter), further in view of IEEE article "Heat Analysis on Insulated Metal Substrates" by Naomi Yunemura et al (Yunemura hereafter).

Regarding Claim 22

Teachings of Sonderman and Jain are disclosed in claim 1 rejection above. Sonderman also teaches that the first principle simulation models the equipment conditions, thereby modeling temperature response and pressure response during various processes (Sonderman: at least in Col.5 Lines 62-67). Jain also teaches distributed and dedicated hardware implementation to solving wafer problem using computer implemented differential equations (Jain: Section III & IV).

Sonderman and Jain do not teach explicitly that such temperature and pressure modeling is done using ANSYS computer code.

Yunemura teaches that heat simulation modeling can be performed using ANSYS computer code (Yunemura: Pg. 1407 Section 1) on a silicon chip.

Motivation to combine Jain with Sonderman is disclosed above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Yunemura to Sonderman and Jain to create a equipment model as disclosed by Sonderman. The motivation to combine would have been that Yunemura teaches heat modeling on a silicon chip

affecting the thermal conductivity (Yunemura: Pg.1407 Section 2) based on various thicknesses and Sonderman is solving the same issue for the equipment model that for example model the equipment for depositing the various layers and affects on heat and pressure. Further, ANSYS is known in art to be used as thermal & pressure modeling tool based on finite element analysis. Motivation to combine Jain and Yunemura is that Jain as taught above indicates distributed solving of computer implemented differential equations which Yunemura solves by ANSYS modeling, thereby facilitating in implementation of Jain's teachings.

Regarding Claim 59

System claim 59 discloses similar limitations as claim 22 and is rejected for the same reasons as claim 22.

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19. Claims 23-28 and 60-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter), further in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter).

Regarding Claims 23-25

Teachings of Sonderman and Jain are disclosed in claim 1 rejection above.

Sonderman and Jain does not explicitly teach close fitting the solution of the first principle simulation run to thereby set initial conditions for cells in the first principle simulation; selecting close fitting solutions from a library based on convergence.

Chen teaches close fitting the solution of the first principle simulation run to thereby set initial conditions for cells in the first principle simulation; selecting close fitting solutions from a library based on convergence (Chen: at least in Col.5 Lines 38 – Col.6 Line 25; Fig 3A-B).

Motivation to combine Jain with Sonderman is disclosed above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Chen to Sonderman and Jain. The motivation to combine would have been that Chen and Sonderman both are analogous art concerned with simulating the semiconductor fabrication process and providing the best control parameters to the actual semiconductor-processing tool (Chen: at least in Col.3 Lines 19-23).

Regarding Claim 26

Chen teaches that the close-fitting solution library existing on a network of computers connected to semiconductor-processing tool (Chen: Fig.2; Col.4 Line 55 –Col.6 Line 19).

Regarding Claims 27-28

Chen teaches calculating solution to the first principle simulation by choosing a coarse grid for solution to the first principle simulation (Chen: at least in Col.6 Line 44-Col.7 Line 14) as user defined parameters; further, subsequent solutions by setting the initial conditions to fine grid are made though Gaussian distribution and actual inline data (Chen: at least in Col.6 Line 46-51).

Regarding Claims 60-62

System claims 60-62 disclose similar limitations as claims 23-35 and are rejected for the same reasons as claims 23-25 respectively.

Regarding Claim 63

System claim 63 discloses similar limitations as claim 26 and is rejected for the same reasons as claim 26.

Regarding Claims 64-65

System claims 64-65 disclose similar limitations as claims 27-28 and are rejected for the same reasons as claims 27-28 respectively.

20. Claims 31, 36, 68 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter), in view of U.S. Patent No. 6,812,045 issued to Mehrdad Nikoonahad (Nikoonahad hereafter).

Regarding Claim 31

Teachings of Sonderman and Jain are disclosed in claim 1 rejection above. Sonderman provides examples of the processing tool as etch and photolithography tools (Col.4 Lines 26-31) but does not explicitly disclose chemical vapor and physical vapor deposition system.

Nikoonahad teaches deposition tools to include chemical vapor and physical vapor deposition system (Nikoonahad: Col.24 Lines 3-49).

Motivation to combine Jain with Sonderman is disclosed above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Nikoonahad to Sonderman and Jain. The motivation to combine would have been that Nikoonahad and Sonderman are analogous art and both are modeling the semiconductor processing and providing feedback to the semiconductor processing tool (Sonderman: Abstract; Nikoonahad: Col.3; Col.93 Lines 20-35).

Regarding Claim 36

Nikoonahad teaches plurality of computing (as processor)/ storage (as memory) devices connected over network to exchange information between a plurality of computing/storage devices including at least one of model solver parameters, solution status to the first principles simulation, model solutions to the first principles simulation, and solution convergence history for said model solutions (Nikoonahad: Col.3 Lines 15-44; Col.68, Lines 41-59).

Regarding Claim 68

System claim 68 discloses similar limitations as claim 31 and is rejected for the same reasons as claim 31.

Regarding Claim 73

System claim 73 discloses similar limitations as claim 36 and is rejected for the same reasons as claim 36.

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21. Claims 35 and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of U.S. Application 10/472,436 filed by David Fatke et al. (Fatke hereafter).

Regarding Claim 35

Teachings of Sonderman and Jain are disclosed in claim 1 rejection above.

Sonderman and Jain do not teach step of controlling by utilizing at least on of non-linear optimization and multivariate analysis to derive the control model for the process control.

Fatke teaches utilizing at least on of non-linear optimization and multivariate analysis to derive the control model for the process control (Fatke: [0011][0012][0035][0050]-[0058][0021]). Fatke uses the partial least square (PLS) model to perform multivariate analysis ([0050] to derive the control model for the process control and provide output to the semiconductor-processing tool ([0021]). Further, Fatke teaches that the nonlinear optimization is known in the art for creating such models ([0012]).

Motivation to combine Jain with Sonderman is disclosed above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Fatke to Sonderman and Jain. The motivation to combine would have been that Fatke and Sonderman are analogous art and Fatke creates a model form the determining the endpoint of the

etching in an etch reactor (Fatke: Abstract/Summary), thereby creating a equipment model and the process model for etching, which can be applied to Sonderman.

Regarding Claim 72

System claim 72 discloses similar limitations as claim 35 and is rejected for the same reasons as claim 35.

Conclusion

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Akash Saxena/

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